RASHTRASANT TUKADOJI MAHARAJ NAGPUR UNIVERSITY

(Established by Government of Central Provinces Education Department by Notification No. 513 dated the 1st of August, 1923 & presently a State University governed by Maharashtra Public Universities Act, 2016)

FACULTY OF SCIENCE AND TECHNOLOGY

DIRECTION NO.12 of 2024

ADMISSION OF STUDENTS AND EXAMINATIONS LEADING TO THE AWARD OF THE DEGREE OF BACHELOR OF APPLIED ELECTRONICS AND SOFTWARE TECHNOLOGY(SEMESTER PATTERN) DIRECTION, 2024

Whereas the Maharashtra Public Universities Act,2016 (Mah.Act No. VI of 2017) (hereinafter the "Act") and the same has been made applicable to the Rashtrasant Tukadoji Maharaj Nagpur University (hereinafter the University")

AND

WHEREAS, the University Grants Commission, New Delhi vide letter No.D.O.No.F-2/2008/(XI Plan), dated 31 January 2008 regarding new initiatives under the XI Plan – Academic reforms in the University has suggested for improving quality of higher education and to initiate the academic reform at the earliest,

AND

Whereas the Special Task Committee for the subject of Applied Electronics Technology, in the former Faculty of Home Science, at its meeting held on 25-8-2016, recommended for starting of semester pattern and prepared the syllabus and scheme of examination for Bachelor of Applied Electronics and Software Technology, programme commensurate with the governing guidelines and also prepared the syllabus and scheme of examination for the said programme for which ultimately Direction No.28 of 2017 was issued;

AND

Whereas, the Special Task Committee for the subject of Applied Electronics Technology in the new Faculty of Science and Technology at its meeting held on 27-11-2018, recommended Amendments to Direction No. 28 of 2017 and prepared the syllabus and scheme of examination for Bachelor of

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Applied Electronics and Software Technology, commensurate with the governing guidelines, to be implemented from academic session 2018-2019,the University had issued Direction No11 of 2019;

AND

Whereas, Direction No. 11 of 2019 entitled "Admission of students and examinations leading to the award of the degree of bachelor of applied electronics and software technology(semester pattern), issued under section12(8) of the Act has lapsed by virtue of the provisions of the proviso to the said provision the necessary Ordinance could not be issued within a period of six months from the date of issuance of the said Direction, necessitating issuance of a new Direction incorporating the provisions of the lapsed Direction No. 11 of 2019 with suitable modifications is bring it in conformity with the standard format of direction governing academic programmes in the University,

Now, therefore, I, Dr. Prashant S. Bokare, Vice Chancellor, Rashtrasant Tukadoji Maharaj Nagpur University, in exercise of my powers under section 12(8) of the Act, do hereby issue the following Direction:

1. This Direction may be called " **Admission of students and examinations leading to the award of the degree of bachelor of applied electronics and software technology(semester pattern) Direction, 2024"**

2. The direction shall come into force from the date of its issuance.

3. In this Direction unless the context otherwise requires:-

    a. **"ATKT"** means "Allowed to Keep Term" in the higher semester, as per the rules herein.

    b. **"Board of Studies"** means Board of studies of the University in the discipline/subjects concerned.

    c. **"Course"** means a theory or practical (or the combination of theory and practical) subject, prescribed for any semester and carrying maximum and minimum passing marks, which a student, admitted to the programme of the Bachelor of Applied Electronics and Software Technology, has to study in order to become eligible for the award of the Degree under this Direction.

    d. **"Credit"** means the unit by which the course work is measured. It is measured in terms of weekly class hours assigned to a Course.

    e. **"Credit Point" (CP):** It is the value obtained by multiplying the Grade Point by the Credit i.e. No. of Credits assigned for the course x Grade Points secured for that course.

f. **"Cumulative Grade Point Average (CGPA)"**: CGPA refers to the Cumulative Grade Point Average weighted across all the semesters. It is obtained by dividing total number of credit points in all the semesters by the total number of credits in all the semesters.

g. **"Degree"** means the Degree of Bachelor of Applied Electronics and Software Technology (Semester Pattern) which is to be awarded to a student admitted to the programme governed by this Direction on successful completion of the programme.

h. **"Grade Letter"**: It is an index to indicate the performance of a student in a particular course/ Paper. It is the transformation of actual marks secured by a student in a course/paper. It is indicated by a Grade letter O, A+,A, B+, B, C, and F. There is a range of marks for each Grade.

i. **"Grade Point"** : Grade Point is the weightage allotted to each grade letter depending on the marks awarded in a course/paper.

j. **"Programme"** means the academic progrogramme consisting of eight semesters, each semester having one or more than one course (subject), leading to the award of the degree of Bachelor of Applied Electronics and Software Technology (Semester Pattern).

k. **"Student"** means student admitted to the Bachelor of Cosmetic Technology (Semester Pattern) programme under this Direction.

l. **Semester Grade Point Average (SGPA)**: SGPA indicates the performance of a student in a given Semester. It is based on the total credit points earned by the student in all the courses and the total number of credits assigned to the courses/papers in a Semester.

m. **"University"**: means Rashtrasant Tukdoji Maharaj Nagpur University, Nagpur

4. The duration of the Bachelor of Applied Electronics and Software Technology course shall be of Four academic years consisting of eight semesters with University examinations at the end of each semester namely:

a. Bachelor of Applied Electronics and Software Technology Semester I Exam.

b. Bachelor of Applied Electronics and Software Technology Semester II Exam.

c. Bachelor of Applied Electronics and Software Technology Semester III Exam.

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d. Bachelor of Applied Electronics and Software Technology Semester IV Exam.

e. Bachelor of Applied Electronics and Software Technology Semester V Exam.

f. Bachelor of Applied Electronics and Software Technology Semester VI Exam.

g. Bachelor of Applied Electronics and Software Technology Semester VII Exam.

h. Bachelor of Applied Electronics and Software Technology Semester VIII Exam.

The period of Academic Session shall be such as may be notified by the university.

5. The Examination specified in paragraph 3 shall be held twice a year at such places on such dates as may be decided by the University. The main examination of semester I,III,V and VII shall be held in winter whereas the examination for semester II,IV,VI and VIII shall be held in summer. The supplementary examination of semester I,III,V and VII will be held in summer whereas supplementary examination for semester II,IV,VI,VIII will be held in winter. There shall be no practical examination during semester I,III,V and VII. Practical examination will be held during semester II,IV,VI,VIII only considering complete curriculum of both the semesters of that particular year.

6. Subject to the compliance with provisions of this Direction and of other ordinances in force from time to time, a candidate for admission to the examination shall:

a.) In case of semester I of Bachelor of Applied Electronics & Software Technology , have passed XII. standard of Maharashtra State Board of Secondary Education or an examination recognized as equivalent there to with Physics, Chemistry, Mathematics and English as subjects or MCVC(Electronics / Electronics Technology or equivalent) from Maharashtra State Board of Secondary Education or equivalent examination.

b) In the case of Bachelor of Applied Electronics & Software Technology Semester III, have passed the Bachelor of Applied Electronics & Software Technology semester I and II Examination of the University or an examination recognized as equivalent there to.

That anyone who holds a First Class Diploma in Electronics and Telecommunications or Diploma in Electronics from any one of the polytechnics in Maharashtra state shall be eligible for admission to third semester of Bachelor of Applied Electronics and Software Technology That any first class diploma holders in Electronics or Electronics and Telecommunication from state other than Maharashtra with English medium alone shall be eligible for admission to the third semester of Bachelor of Applied Electronics and Software Technology course provided equivalence of diploma examination passed by him/her from polytechnic in other state is established by the university

c) In the case of Bachelor of Applied Electronics & Software Technology semester V, have passed the Bachelor of Applied Electronics & Software Technology semester I,II, III, IV Examination of the University or an examination recognized as equivalent there to.

d) In the case of Bachelor of Applied Electronics & Software Technology semester VII, have passed the Bachelor of Applied Electronics & Software Technology semester I,II,III,IV, V,VI Examination of the University or an examination recognized as equivalent there to.

7. A student shall undergo 'Industrial Training' after appearing at the IV th Semester of Bachelor of Applied Electronics and Software Technology culminating to a total of 6 weeks in any Industry and shall produce a certificate to that effect to the satisfaction of the Principal of the College.

8. a) Without prejudice to the other provisions of the Ordinance No. 6 relating to the examination in general the provision of paragraph 5,7,8,10 and 32 of the said ordinance shall apply to every collegiate candidate.
   b) The ATKT rules for admission for the Course Bachelor of Applied Electronics and Software Technology (Theory and Practical as separate passing head) shall be as given in the following table

Admission to semester	Candidate should have passed in all the subjects of the following examination of R.T.M. Nagpur University	Candidate should have passed at least half of the total passing heads taken together prescribed for Examinations given below (on calculation, fraction if any should be Ignored)	Candidate should have appeared for the following examinations
Semester I	As provided in the para 5 of the Direction	----------	------------------
Semester II	----------	----------	
Semester III	----------		Semester I
Semester IV	----------	Semester I and II	
Semester V	Semester I and II	----------	Semester III
Semester VI	----------	Semester III and IV	
Semester VII	Semester III and IV	------------------	Semester V
Semester VIII	------------------	Semester V and VI	
		------------	Semester VII

9. The fees for the examinations shall be as prescribed by the University, from time to time and whenever, any change is made in the fees prescribed for any particular examination that shall be notified through a notification for the information of all concerned.

Credit and Grade Point System

Conversion of Marks to Grades and Calculations of SGPA (Semester Grade Point Average) and CGPA (Cumulative Grade Point Average):

In the Credit and Grade Point System, the assessment of individual courses in the concerned examinations will be on the basis of marks only, but the marks will later be converted in Grades by a mechanism wherein the overall performance of the candidates shall be reflected after considering the Credit Points for any given course. However, the overall evaluation shall be designated in terms of Grade.

Abbreviations and formulae

G: Grade

GP: Grade Points

C: Credits

CP: Credit Points

CG: Credits x Grades (Product of Credits and Grades)

SGPA: Semester Grade Point Average shall be calculated for individual semesters

SGPA = $\sum$CG: Sum of product of Credits and Grade Point/$\sum$C: Sum of Credit Points

CGPA: Cumulative Grade Points Average shall be calculated for the entire programme by considering all the semesters taken together.

CGPA to Percentage: Percentage (%) = (CGPA)*10

After calculating the SGPA for an individual semester and the CGPA for the entire programme, the value can be matched with the grade in the Grade Point Table as per the 10 (ten) Point Grading System and expressed as a single designated Grade such as O, A, B, C, D, P and F.

Sr. No.	Letter Grade	Grade Points	Marks Range	Performance
01.	O	10	Above 90 up to 100	Outstanding
02.	A+	9	Above 80 up to 90	Excellent
03.	A	8	Above 70 up to 80	Very Good
04.	B+	7	Above 60 up to 70	Good
05.	B	6	Above 55 up to 60	Above Average
06.	C	5	Above 50 up to 55	Average
07.	P	4	40 to 50	Pass
08.	F	0	Below 40	Fail
09.	AB	0	Absent	Fail

A student obtaining Grade F shall be considered Fail and will be required to re-appear in the examination.

Division at the Bachelor of Applied Electronics and Software Technology examination shall be declared on the basis of the aggregate marks of Bachelor of Applied Electronics and Software Technology Semester I and Semester VIII examination taken together and the CGPA will be calculated and notified. The successful examinees at the BAE&ST Semester VIII examination shall be

awarded division on the basis of CGPA. The percentage of passing marks in each subject shall be as indicated in the Scheme of Examination (Appendix A).

Criteria for Class / Final Grade:

CGPA	Class/ Division
7.50 to 10.00	First Class with Distinction
6.00 to 7.49	First Class
5.00 to 5.99	Second Class
4.00 to 4.99	Third Class

10. Every candidate for Bachelor of Applied Electronics & Software Technology Semester I,II,III,IV,V,VI,VII,VIII Examination shall be examined in the subjects as set out in the Appendix to Directions

    i. The scope of the subjects shall be as indicated in the respective syllabus in force from time to time.

    ii. Medium of examination shall be English.

11 .An applicant for admission to an Examination shall satisfy the Head of the Department / Principal as regards the Sessional examinations/Internal assessment conducted during the academic year regarding her / his suitability to take the University examination.

12. In order to pass in the Examination an examinee shall obtain in each subject not less than the minimum marks as indicated in the Appendix 1,2,3,4,5,6,7,8.

13. The Head of the Department / Principal shall maintain in her/his office the complete record of the marks obtained by the candidate in the Sessional examinations/internal assessment that shall be submitted, before the commencement of the University examination, to the Director of Examination, in a sealed cover.

14. There shall be no classification of successful examinees at I,II,III,IV,V,VI,VII semesters of Bachelor of Applied Electronics and Software Technology. Division of examinees successful at the VIII [th] semester of Bachelor of Applied Electronics and Software Technology shall be determined on the basis of the aggregate marks obtained at all the semesters of Bachelor of Applied Electronics & Software Technology.

15. Those obtaining 60% or more marks in aggregate shall be placed in First Division and all other successful examinees in the Second Division respectively.

16. An examinee who is successful at an examination and obtained not less than 75% or more of the marks prescribed in a subject shall be declared to have passed the examination with Distinction in that subject.

17. Provision of Ordinance No. 7 A – relating to the condonation of Deficiency of marks for passing an examination and of ordinance No. 10 relating to examinations and compartments as amended from time to time shall apply to the Examination under this direction.

18. An unsuccessful examinee at any of the examination of Bachelor of Applied Electronics & Software Technology shall have an option to carry her/his Sessional Examination/Internal assessment college assessment marks for Theory/Practical examinations to her/his successive attempt(s) at the examination. The examinee however can forgo her/his Sessional Examination/Internal assessment marks in subject/subjects in which case she/he shall be examined for total marks comprising of theory /practical and college assessment together at her/his successive attempt(s).

19. As soon as possible after the examinations but not later than 30th June next following in case of examination held in March-April and 26th February next following, in case of examination held in October-November, the Board of Exams shall publish a list of successful examinees. List of successful examinees at the Eighth semester of Bachelor of Applied Electronics & Software Technology examination shall be arranged in the First and Second Division as envisaged in clause 14 of the ordinance and names of examinee passing the said examination as whole in the minimum prescribed period and obtaining the prescribed number of places in the first or second Division shall be arranged in order of Merit as provided in the examination in General Ordinance No. 6.

20. Notwithstanding anything to the contrary in this direction, no person shall be admitted to this examination, if she/he already passed the same examination or an equivalent examination thereto of other statutory university.

21. That educational tour or visit comprising of 1-5 days shall be compulsory to the students at least once during four years of the course.

22. Successful examinees at the I,II,III,IV,V,VI,VII,VIII semesters of Bachelor of Applied Electronics and Software Technology Examination shall be entitled to receive certificate signed by Registrar, titled Bachelor of Applied Electronics and Software Technology, Semester I, II, III , IV,V,VI,VII,VIII respectively and those successful at all the exams of Bachelor of Applied Electronics & Software Technology shall on payment of the prescribed fee receive a degree in the prescribed form, signed by the Vice-Chancellor, at the convocation to be held by the University.

23. The Scheme of Examination shall be as per Appendix: 1,2,3,4,5,6,7 and 8 (Semester pattern). The details / title of the theory papers can be suitably modified considering the need of the subject without disturbing the main structure.

24. In the event of any dispute arising under this Direction or should any question of interpretation of any provision of this Direction arise the same shall be referred to the Vice-Chancellor who shall decide the issue in consultation with the dean, Faculty of Science and Technology and the decision of the Vice-Chancellor shall be final and binding on all concerned people.

(Dr. Prashant S. Bokare)
Vice-Chancellor

Nagpur:-
Date:- 12-3-2024

APPENDIX 1
(Semester Pattern)

BACHELOR OF APPLIED ELECTRONICS & SOFTWARE TECHNOLOGY UNDER THE FACULTY OF HOME SCIENCE

Semester I

Sr. No.	Subjects	Maxi-mum Sessional	Marks Paper/ Pract.	Total	Passing Marks	No. of Periods		Exam Time Hrs.
						TH	PR	
1-T-1	Applied Physics	10	40	50	20	4		2
1-P-1	**Applied Physics**		-				3	
1-T-2	Applied Chemistry	10	40	50	20	4		2
1-P-2	**Applied Chemistry**						3	
1-T-3	Computer Programming I	10	40	50	20	4		2
1-P-3	**Computer Programming I**						3	
1-T-4	Electrical Engineering	10	40	50	20	4		2
1-P-4	**Electrical Engineering**						3	
1-T-5	Engineering Mathematics I	10	40	50	20	4		2
1-T-6	Social Science	10	40	50	20	4		2
1-P-5	**Communicative English**						3	
1-P-6	**Engineering Drawing I**						6	
	Total Marks			300		24	21	

One practical batch will consists of 12-16 students.

APPENDIX 2

BACHELOR OF APPLIED ELECTRONICS & SOFTWARE TECHNOLOGY UNDER THE FACULTY OF HOME SCIENCE Semester II

Sr. No.	Subjects	Maxi-mum Sessional	Marks Paper/ Pract.	Total	Passing Marks	No. of Periods		Exam Time Hrs.
						TH	PR	
2-T-1	Applied Physics	10	40	50	20	4		2
2-P-1	Applied Physics	20	80	100	50		3	3
2-T-2	Applied Chemistry	10	40	50	20	4		2
2-P-2	Applied Chemistry	20	80	100	50		3	3
2-T-3	Computer Programming I	10	40	50	20	4		2
2-P-3	Computer Programming I	20	80	100	50		3	3
2-T-4	Electrical Engineering	10	40	50	20	4		2
2-P-4	Electrical Engineering	20	80	100	50		3	3
2-T-5	Engineering Mathematics I	10	40	50	20	4		2
2-T-6	Social Science	10	40	50	20	4		2
2-P-5	Communicative English	20	80	100	50		3	3
2-P-6	Engineering Drawing I	20	80	100	50		6	3
	Total Marks:			900		24	21	

One practical batch will consist of 12-16 students.

APPENDIX 3

BACHELOR OF APPLIED ELECTRONICS & SOFTWARE TECHNOLOGY UNDER THE FACULTY OF HOME SCIENCE

Semester III

Sr. No.	Subjects	Maxi- mum Sess- ional	Marks Paper/ Pract.	Total	Passing Marks	No. of Periods		Exam Time Hrs.
						TH	PR	
3-T-1	Electron Devices and Circuits	10	40	50	20	4		2
3-P-1	**Electron Devices and Circuits**						3	
3-T-2	Digital Electronics	10	40	50	20	4		2
3-P-2	**Digital Electronics**						3	
3-T-3	Computer Programming II	10	40	50	20	4		2
3-P-3	**Computer Programming II**						3	
3-T-4	Engineering Mechanics	10	40	50	20	4		2
3-P-4	**Engineering Drawing II**						3	
3-T-5	Linear Network Analysis	10	40	50	20	4		2
3-T-6	Engineering Mathematics II	10	40	50	20	4		2
3-P-5	**Workshop**						3	
	Total Marks			300		24	15	

One practical batch will consist of 12-16 students.

APPENDIX 4

BACHELOR OF APPLIED ELECTRONICS & SOFTWARE TECHNOLOGY UNDER THE FACULTY OF HOME SCIENCE

Semester IV

Sr. No.	Subjects	Maxi-mum Sess-ional	Marks Paper/ Pract.	Total	Passing Marks	No. of Periods		Exam Time Hrs.
						TH	PR	
4-T-1	Electron Devices and Circuits	10	40	50	20	4		2
4-P-1	**Electron Devices and Circuits**	20	80	100	50		3	3
4-T-2	Digital Electronics	10	40	50	20	4		2
4-P-2	**Digital Electronics**	20	80	100	50		3	3
4-T-3	Computer programming II	10	40	50	20	4		2
4-P-3	**Computer programming II**	20	80	100	50		3	3
4-T-4	Engineering Mechanics	10	40	50	20	4		2
4-P-4	**Engineering Drawing II**	20	80	100	50		3	3
4-T-5	Linear Network Analysis	10	40	50	20	4		2
4-T-6	Engineering Mathematics II	10	40	50	20	4		2
4-P-5	**Workshop**	20	80	100	50		3	3
	Total Marks			800		24	15	

One practical batch will consist of 12-16 students.

APPENDIX 5

BACHELOR OF APPLIED ELECTRONICS & SOFTWARE TECHNOLOGY UNDER THE FACULTY OF HOME SCIENCE

Semester V

Sr. No.	Subjects	Maxi-mum Sess-ional	Marks Paper/ Pract.	Total	Passing Marks	No. of Periods		Exam Time Hrs.
						TH	PR	
5-T-1	Linear Integrated Circuits	10	40	50	20	4		2
5-P-1	**Linear Integrated Circuits**						3	
5-T-2	Microcontrollers	10	40	50	20	4		2
5-P-2	**Microcontrollers**						3	
5-T-3	Instrumentation and Control Systems	10	40	50	20	4		2
5-P-3	**Instrumentation and Control Systems**						3	
5-T-4	Digital Signal Processing	10	40	50	20	4		2
5-P-4	**Digital Signal Processing**						3	
5-T-5	Algorithm and Data Structure	10	40	50	20	4		2
5-P-5	**Algorithm and Data Structure**						3	
5-T-6	Communication Electronics	10	40	50	20	4		2
	Total Marks			300		24	15	

APPENDIX 6

BACHELOR OF APPLIED ELECTRONICS & SOFTWARE TECHNOLOGY UNDER THE FACULTY OF HOME SCIENCE

Semester VI

Sr. No.	Subjects	Maxi-mum Sess-ional	Marks Paper/ Pract.	Total	Passing Marks	No. of Periods TH	No. of Periods PR	Exam Time Hrs.
6-T-1	Linear Integrated Circuits	10	40	50	20	4		2
6-P-1	**Linear Integrated Circuits**	20	80	100	50		3	3
6-T-2	Microcontrollers	10	40	50	20	4		2
6-P-2	**Microcontrollers**	20	80	100	50		3	3
6-T-3	Instrumentation and Control Systems	10	40	50	20	4		2
6-P-3	**Instrumentation and Control Systems**	20	80	100	50		3	3
6-T-4	Digital Signal Processing	10	40	50	20	4		2
6-P-4	**Digital Signal Processing**	20	80	100	50		3	3
6-T-5	Algorithm and Data Structure	10	40	50	20	4		2
6-P-5	**Algorithm and Data Structure**	20	80	100	50		3	3
6-T-6	Communication Electronics	10	40	50	20	4		2
	Total Marks			800		24	15	

APPENDIX 7

BACHELOR OF APPLIED ELECTRONICS & SOFTWARE TECHNOLOGY UNDER THE FACULTY OF HOME SCIENCE

Semester VII

Sr. No.	Subjects	Maximum Sessional	Marks Paper/ Pract.	Total	Passing Marks	No. of Periods TH	No. of Periods PR	Exam Time Hrs.
7-T-1	Circuit Design	10	40	50	20	4		2
7-P-1	**Circuit Design**						3	
7-T-2	Advanced Microcontrollers	10	40	50	20	4		2
7-P-2	**Advanced Microcontrollers**						3	
7-T-3	System Design	10	40	50	20	4		2
7-P-3	**System Design**						3	
7-T-4	Advanced Programming	10	40	50	20	4		2
7-P-4	**Advanced Programming**						3	
7-T-5	Industrial Organisation & Management	10	40	50	20	4		2
7-T-6	Data Base Management system	10	40	50	20	4		2
7-P-5	**Project**						3	
	Total Marks			300		24	15	

One practical batch will consist of 12-16 students.

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APPENDIX 8

BACHELOR OF APPLIED ELECTRONICS & SOFTWARE TECHNOLOGY UNDER THE FACULTY OF HOME SCIENCE

Semester VIII

Sr. No.	Subjects	Maxi-mum Sess-ional	Marks Paper/ Pract.	Total	Passing Marks	No. of Periods		Exam Time Hrs.
						TH	PR	
8-T-1	Circuit Design	10	40	50	20	4		2
8-P-1	**Circuit Design**	20	80	100	50		3	3
8-T-2	Advanced Microcontrollers	10	40	50	20	4		2
8-P-2	**Advanced Microcontrollers**	20	80	100	50		3	3
8-T-3	System Design	10	40	50	20	4		2
8-P-3	**System Design**	20	80	100	50		3	3
8-T-4	Advanced Programming	10	40	50	20	4		2
8-P-4	**Advanced Programming**	20	80	100	50		3	3
8-T-5	Industrial organisation & Management	10	40	50	20	4		2
8-T-6	Elective	10	40	50	20	4		2
8-P-5	**Project**	20	80	100	50		3	3
	Total Marks			800		24	15	

Elective (8-T-6) :i) Computer Network ii) Mobile Communication iii) Television

One practical batch will consists of 12-16 students.

Appendix - 9

Bachelor of Applied Electronics and Software Technology

(Semester Pattern)

Instructions to Examiners

Every Theory paper consists of five units. Theory examination conducted by university in each subject will be of 40 marks in every semester. Examination for each theory paper will be of two hours.

There must be one question on each unit (Total five questions) and two questions will be mixed questions based on complete syllabus. Thus Examiner/Paper setter should set total seven questions of eight marks each.

Examiner can set questions of eight marks or can divide question in two parts a and b of four marks each.

APPENDIX 10

BACHELOR OF APPLIED ELECTRONICS AND SOFTWARE TECHNOLOGY
Absorbtion Scheme

Absorbtion scheme to transfer from Bachelor of Applied Electronics and Software Technology yearly pattern to from Bachelor of Applied Electronics and Software Technology semester pattern can be implemented as below:

Student who has passed all the subjects of first year(yearly pattern) should be directly allowed to take admission to third semester of new course.

Student who has passed all the subjects of first year(yearly pattern) and second year (yearly pattern)should be directly allowed to take admission to fifth semester of new course.

Student who has passed all the subjects of first year, second year and third year (yearly pattern) should be directly allowed to take admission to seventh semester of new course.

In the interest of the students , students of old course(yearly pattern) may be allowed 1+5 chances to pass the subjects of the concerned year , after commencement of new course (semester pattern).

If an examinee failed to pass the under graduate programme within EIGHT successive years (for Eight semesters degree) from the date of his / her first admission to particular programme he/ she shall be declared as "Not Fit for the Course (NFC)" and he/ she will not be allowed to appear further for any previous examination of the course.

EQUIVALENCE FOR YEARLY TO SEMESTER PATTERN

YEAR	Paper	OLD	Paper	NEW	REMARKS/ JUSTIFICATION
Part-I	1-T-1	Applied Physics	1-T-1 2-T-1	Applied Physics	
	1-P-1	Applied Physics	1-P-1 2-P-1	Applied Physics	
	1-T-2	Applied Chemistry	1-T-2 2-T-2	Applied Chemistry	
	1-P-2	Applied Chemistry	1-P-2 2-P-2	Applied Chemistry	
	1-T-3	Electrical Engineering	1-T-4 2-T-4	Electrical Engineering	
	1-P-3	Electrical Engineering	1-P-4 2-P-4	Electrical Engineering	

	1-T-4	C Programming	1-T-3	Computer Programming I	
			2-T-3		
	1-P-4	C Programming	1-P-3	Computer Programming I	
			2-P-3		
	1-T-5	Engineering Mathematics-I	1-T-5	Engineering Mathematics I	
			2-T-5		
	1-T-6	Social Science	1-T-6	Social Science	
			2-T-6		
	1-P- 5	Engineering Drawing	1-P-6	Engineering Drawing I	
	1-P- 6	Communicative English	1-P-5	Communicative English	

YEAR	Paper	OLD	Paper	NEW	REMARKS/ JUSTIFICATION
Part-II	2-T-1	Electron Devices & Circuits	3-T-1	Electron Devices & Circuits	
			4-T-1		
	2-P-1	Electron Devices & Circuits	4-P-1	Electron Devices & Circuits	
	2-T-2	Measurements &Measuring Instruments			Modified and advancement in the subject are covered in 5S-T-3 and 6S-T-3
	2-P-1	Measurements &Measuring Instruments			
	2-T-3	Engineering Mechanics	3-T-4	Engineering Mechanics	
			4-T-4		

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	2-P-3	Engineering Mechanics	3-P-4 4-P-4	Engineering Drawing II	
	2-T-4	Algorithms & Data Structures	--	-----	
	2-T-4	Algorithms & Data Structures	-----	-----	
	2-T-5	Digital Electronics	3-T-2 4-T-2	Digital Electronics	
	2-P-5	Digital Electronics	3, 4-P-2	Digital Electronics	
	2-T-6	Engineering Mathematics-II	3-T-6 4-T-6	Engineering Mathematics	
	2-T-7	Linear Network Analysis	3-T-3 4-T-3	Linear Network Analysis	
	2-P-6	Workshop	3,4-P-5	Workshop	

YEAR	Paper	OLD	Paper	NEW	REMARKS/ JUSTIFICATION
Part – III	3-T-1	Instrumentation & Control Systems	5-T-3 6-T-3	Instrumentation & Control Systems	
	3-P-1	Instrumentation & Control Systems	5,6-P-3	Instrumentation & Control Systems	
	3-T-2	Linear Integrated Circuits	5-T-1 6-T-1	Linear Integrated Circuits	

	3-P-2	Linear Integrated Circuits	5,6-P-1	Linear Integrated Circuits	
	3-T-3	Microprocessor Techniques			Modified and advancement in the subject are covered in 5-T-2 and 6-T-2
	3-P-3	Microprocessor Techniques			Modified and advancement in the subject are covered in 5-P-2 and 6-P-2
	3-T-4	Communication Electronics	5-T-6 6-T-6	Communication Electronics	
	3-P-4	Communication Electronics			
	3-T-5	Object Oriented Programming	5-T-5 6-T-5	Computer Programming II	
	3-P-5	Object Oriented Programming	5-P-5 6-P-5	Computer Programming II	
	3-T-6	Digital Signal Processing	5,6-T-4	Digital Signal Processing	
	3-P-6	Digital Signal Processing	5-P-4 6-P-4	Digital Signal Processing	
	3-T-7	Computer Organisation			Modified and advancement in the subject are covered in 7-T-6

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YEAR	Paper	OLD	Paper	NEW	REMARKS/ JUSTIFICATION
Part-IV	4-T-1	Circuit Design	7-T-1 8-T-1	Circuit Design	
	4-P-1	Circuit Design	7,8-P-1	Circuit Design	
	4-T-2	Advanced Programming	7-T-4 8-T-4	Advanced Programming	
	4-P-2	Advanced Programming	7,8-P-4	Advanced Programming	
	4-T-3	Digital Communication	5-T-6 6-T-6	Communication Electronics	
	4-T-4	Industrial Organisation & Management	7-T-5 8-T-5	Industrial Organisation & Management	
	4-T-5	Microcontrollers	5-T-2 6-T-2	Microcontrollers	
	4-P-5	Microcontrollers	6-P-2	Microcontrollers	
	4-T-6	System Design	7-T-3 8-T-3	System Design	
	4-P-6	System Design	7,8-P-3	System Design	
	4-P-3	Software Project	7,8-P-5	Project	
	4-P-4	Hardware Project	7,8-P-5	Project	

NOTE: There is no change in the teaching workload.